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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,446	01/12/2004	Theodore Carter Briggs	200313645-1	2130

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,446	BRIGGS ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,10-16 and 18* is/are rejected.

7)☒ Claim(s) *3,4,7-9 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Status

1. This Office Action is in response to applicant's communication filed April 10, 2007 in response to the PTO Office Action mailed January 30, 2007. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claim 16 has been amended, and no claims have been canceled or added. Claims 1-18 remain pending in this application.

Response to Arguments

3. Applicant's arguments filed April 10, 2007 have been fully considered and some have been determined to be persuasive.

In response to the argument that House (US Patent 4,796,232) "servers no function in a system having only a single processor, and is not applicable with regard to a system having a plurality of independent memories", applicant is arguing limitations that do not exist in the claim language. There is no mention of any limitations concerning number of processors or independent memories. Therefore, this argument is not persuasive.

Examiner agrees with applicant's argument that House fails to disclose transferring read and write memory data between the memory controller and buffers and buffering data between the memory controller and system memory for claim 12, and new grounds of rejection are provided below.

Examiner agrees with applicant's argument that House fails to disclose fanning memory address information received in the buffer to more than one system memory bus in light of applicant's amendment of claim 16, and new grounds of rejection are provided below.

Examiner agrees with applicant's argument that Platko fails to disclose a connection between the buffer and a random access memory bus for claim 1, and new grounds of rejection are provided below.

Examiner agrees with applicant's argument that Fortuna fails to disclose a second buffer between the controller and system memory serving as a tag buffer or a tag interface control bus between the memory controller and the tag buffer, and new grounds of rejection are provided below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5-6, 10-12, 15-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over House (US Patent No. 4,796,232) in view of Bao (US PGPub 20010052060).

For claim 1, House discloses a memory control apparatus in a computing system comprising:

a memory controller and a buffer (fig. 1, items 40-48, 50-53, 70-73);

said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller (data buffers... include a data bus input, a memory data bus output and a control signal input, col. 5, lines 10-16; fig. 1, items 60-63, 80-83, 40-48; a dual port memory controller which includes a dedicated logic array coupled to an arbitrator system, col. 4, lines 6-8);

and a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory (a memory array includes... individual memory banks, all of which are commonly coupled to a memory data bus terminal, where the memory is constructed in accordance with conventional dynamic RAM memories, col. 4, lines 47-55; fig. 1, items 11-16).

House fails to disclose the remaining claim limitations.

Bao discloses a memory controller and buffer being connected by a bidirectional data bus and a control interface (fig. 1, items 23, 25, 31, 35, 37);

and said buffer being connected to a random-access memory bus for read and write operations (fig. 1, items 19, 31, 35).

House and Bao are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Bao suggests that it would have been desirable to incorporate a bidirectional data bus and random-access memory bus into the system of Bao because this would provide a system that reduces the load imposed on the system bus by write operations (par. 0008). Therefore, it would have

been obvious to a person of ordinary skill in the art at the time the invention was made to modify House as suggested by Bao to incorporate the feature as claimed.

For claim 5, House discloses the control interface between the memory controller and buffer comprises a memory interface address bus for transferring memory addresses from the memory controller to the buffer (House: fig. 1, port_A and port_B address buses).

For claim 6, House discloses the control interface between the controller and buffer comprises a memory interface control bus for transferring memory control commands from the controller to the buffer (House: fig. 1, port control A, port control B).

For claim 10, House discloses the buffer comprises control logic for decoding memory interface control commands (House: col. 4, lines 6-8).

For claim 11, House discloses the buffer comprises multiple data and control interfaces to system memory, one to interface with each independent portion of system memory (fig. 1).

For claim 12, House discloses a method for data transfer between a memory controller and a system memory bus connected to a system memory in a computing system comprising:

providing to a buffer memory interface addresses and memory interface control commands to facilitate said buffer's read and write operations from and to a system memory (fig. 1, items 40-48, 50-53, 70-73);

addressing said system memory through said buffer to accomplish read and write operations between the system memory and the memory controller (fig. 1, items 40-48, 50-53, 70-73);

decoding in said buffer the memory interface control commands (col. 4, lines 6-8).

House fails to disclose interposing the buffer between the system memory bus and the memory controller;

temporarily storing data read and write memory data in the buffer during data transfer between the system memory and the buffer; and

transferring read and write memory data between said memory controller and said buffer during read and write operations.

Bao discloses a computer system with a system-bus buffer for buffering memory-access requests including read and write requests, where the system-bus buffer stores address, content and control data (par. 0009, 0022; fig. 1, items 19, 23, 25, 31, 35, 37).

House and Bao are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Bao suggests that it would have been desirable to incorporate interposing the buffer between the system memory bus and the memory controller and storing and transferring read and write memory data to and from the buffer into the system of House because this would provide a system that reduces the load imposed on the system bus by write operations (par. 0008). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to modify House as suggested by Bao to incorporate the feature as claimed.

For claim 15, House discloses controlling read and write operations to said system memory with the decoded memory interface control commands originating in the memory controller and decoded in the buffer (a request by a pcoessor is applied to terminal of gate array and an appropriate address is applied to an address buffer while data is received through a data buffer, col. 6, lines 53-64; a write control is coupled to terminal of gate array by a processor and an address is coupled to address buffer while the desired data to be stored is applied to data buffer, col. 6, lines 65-68, col. 7, lines 1-3; fig. 1).

For claim 16, House and Bao disclose fanning memory address information received in the buffer from the controller to the system memory through a data address control bus connecting the buffer to more than one system memory bus (House: fig. 1, port_A and port_B address buses; Bao: the favored contexts include systems with multiple processors, systems with multiple memory controllers, and, more generally, systems with system buses involved in may different types of data transfers, par. 0014).

For claim 18, House discloses a memory control apparatus in a computing system comprising:

a memory controller and a means for buffering data between said controller and system memory (fig. 1, items 40-48, 50-53, 70-73);

said buffer means comprising means for temporarily storing data exchanged between the memory controller and system memory, said buffer means further

comprising logical circuits to decode memory interface control commands from said memory controller (col. 5, lines 10-16; fig. 1, items 60-63, 80-83, 40-48; col. 4, lines 6-8);

and a data access and control bus connected between the buffer and a random-access memory bus to control read and write operations from and to system memory (fig. 1, items 11-33, 60-63, 80-83, 40-48).

House fails to disclose the remaining claim limitations.

Bao discloses a memory controller and a buffer means being connected by a bidirectional data bus and a control interface (fig. 1, items 23, 25, 31, 35, 37); and

said buffer means being connected to multiple random-access memory busses for read and write operations (fig. 1, items 19, 31, 35; par. 0014).

House and Bao are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Bao suggests that it would have been desirable to incorporate a bidirectional data bus and multiple random-access memory bussesinto the system of Bao because this would provide a system that reduces the load imposed on the system bus by write operations (par. 0008). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify House as suggested by Bao to incorporate the feature as claimed.

6. Claims 2 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over House (US Patent No. 4,796,232) in view of Bao (US PGPub 20010052060) and further in view of Liencres et al (US Patent 5,765,196).

For claim 2, House and Bao fail to disclose a second buffer serving as a tag buffer, said second buffer being connected to said random-access memory bus for read and write operations;

said second buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller;

a data access and control bus connected between the tag buffer and the system memory to control read and write operations from and to system memory.

Liencres discloses a multi-processor computing system utilizing a buffer along with a plurality of tag buffers, where each central processor is connected via system address and control buses to a main memory and a system controller (col. 2, lines 47-53; fig. 2, items 108, 110, 210, 220; fig. 4, items 110, 210, 415-440).

House, Bao and Liencres are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Liencres suggests that it would have been desirable to incorporate a tag buffer into the combined system of House and Bao because this would improve the copyback performance in a multi-processor computing system (col. 2, lines 47-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify House and Bao as suggested by Liencres to incorporate the feature as claimed.

For claim 13, House and Bao fail to disclose interposing a second buffer between the controller and system memory serving as a tag buffer.

Liencres discloses a multi-processor computing system utilizing a buffer along with a plurality of tag buffers, where each central processor is connected via system address and control buses to a main memory and a system controller (col. 2, lines 47-53; fig. 2, items 108, 110, 210, 220; fig. 4, items 110, 210, 415-440).

House, Bao and Liencres are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Liencres suggests that it would have been desirable to incorporate a tag buffer into the combined system of House and Bao because this would improve the copyback performance in a multi-processor computing system (col. 2, lines 47-48). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify House and Bao as suggested by Liencres to incorporate the feature as claimed.

For claim 14, House, Bao and Liencres disclose updating memory tag information through a tag interface control bus between the memory controller and the tag buffer (system interface connects a bi-directional data bus to the inbound and outbound queues [of the address controller] and for transfer of data between the data controller and other elements in the multi-processor computer system, col. 4, lines 30-33; fig. 4, items 110, 210).

Allowable Subject Matter

7. Claims 3-4, 7-9 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

When responding to this Office Action:

8. Applicant is requested to indicate where in the disclosure support is to be found for any new language added to the claims by amendment. 37 C.F.R. § 1.75(d)(1) requires such support in the Specification for any new language added to the claims and 37 C.F.R. § 1.83(a) requires support be found in the Drawings for all claimed features.

Applicant must clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made, and must also explain how the amendments avoid the references or objections. See 37 C.F.R. § 1.111(c).

Contact Information

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DIC

7-3-07

STEPHEN C. ELMORE
PRIMARY EXAMINER